AUTOMATIC CONTROL and COMPUTER SCIENCE Section

CONTENTS

Cross-organizational Compatibility Detection with Process Minin
Maria Laura Sebu and Horia Ciocârlie

Full text

Current paper presents an analysis over inter-organizational collaboration in different forms and offers a process based solution for the identification of compatibility in between organizations. The most compatible organizations detected will ensure the premises for a successful collaboration and better business results. Process mining techniques and graph comparison algorithms are used for this purpose. After extracting process definitions of all possible organizations, the business processes are reduced to graph format. Graphs are compared and a process similarity metric is calculated. For graph comparison node match, syntactic and semantic algorithms are implemented and evaluated. In this study we perform an analysis of the failures causes and we identify how the process similarity metric could help overcoming the limitations and ensure a good collaboration start for the organizations. The theoretical aspects are illustrated on a case study, business processes used in different organizations for the same business case. The algorithm evaluation results cover execution time, precision, memory, preconditions.

Key words: organizational collaboration; process similarity; business process management; process mining.
2010 Mathematics Subject Classification: 05C85, 90C59.

top

Improving the Predictability of nMPRA and nHSE Architecture
Nicoleta Cristina Gaitan, Ionel Zagan and Vasile Gheorghita Gaitan

This paper describes a multithreaded CPU implementation based on a hardware scheduler engine and four stage pipeline architectures. The major problems for operating systems are represented by task switching with significant delays and the synchronization and communication between tasks. In consequence, this can affect deadline requirements for hard real-time applications. Our architecture provides a fast task switching time and executes all instruction without flushing the pipeline. This will increase the predictability of the processor by removing the hazard unit. To achieve this, we propose a multithreading processor with an innovative pipeline architecture and a particular preemptive scheduler implemented in the hardware. This implementation enables multiple threads to share a single pipeline datapath with a simplified task context switch.

Key words: hardware multithreading; pipeline processing; hardware scheduler; real-time; embedded systems.

2010 Mathematics Subject Classification: 97P60, 65Y10.

Determination of Initial Basic Feasible Solution of a Transportation Problem: A TOCM-SUM Approach
Aminur Rahman Khan, Adrian Vîlcu, Nahid Sultana and Syed Sabbir Ahmed

A new heuristic for obtaining an initial basic feasible solution of a transportation problem (TP) is introduced in this paper. The proposed method is illustrated with a number of numerical examples. Comparison of findings obtained by the new heuristic and the existing heuristics show that the method presented herein gives a better result.

Key words: VAM; MMM; TOCM; HCDM; Pointer cost; Optimum solution.

2010 Mathematics Subject Classification: 90B50, 90C08.

Study of Metastability in Digital Systems
Călin Mircea Monor, Mihai Timiş and Alexandru Valachi

In this paper, the authors propose a study of the metastability in digital systems. We develop a comprehensive study for the metastability and propose a new algorithm in order to reduce it in the digital systems. Our proposed idea is to add a regular two-flop synchronizer. Also an experimental system and method for measuring synchronizers and metastable flip-flops are described. The regular synchronizer is useful for communications between asynchronous clock domains, while the other synchronizers can provide higher bandwidth communications between synchronous systems.

Key words: metastability, digital systems, finite state machine, asynchronous inputs synchronization, hazard in digital systems.

2010 Mathematics Subject Classification: 06E30, 49M27, 94C05.

Boolean Function Decomposition Based on FPGA Basic Cell Structure
Călin Mircea Monor and Alexandru Valachi

The authors present a method for the decomposition of Boolean functions starting from the structure of the basic cell of the FPGA technologies. Starting from a general method of implementing Boolean functions, the authors develop a new method of decomposition using sub-functions that can be synthesized using one single FPGA basic cell. The general method proves that there is a solution for implementing a Boolean function with a given number of variables. The method presented in the current paper provides, if it exists, an optimization of the general result. If the optimized solution exists, it will be working at higher frequency and, eventually, it will require a smaller number of basic cells for implementation.

Key words: Boolean function; decomposition; sub-function; basic cell; FPGA; LUT; frequency optimization; area optimization.

2010 Mathematics Subject Classification: 06E30, 49M27, 94C05.